Docket No. IRV1.PAU.30 **Patent Application**

#13 Declaration Jmeinthe 9/11/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :	Examiner: D. Graybill
Douglas M. Albert et al.	Group Art Unit: 3722
Serial No.: 09/190,378	
Filed: November 10, 1998	
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine, California
	October 22, 2001

DECLARATION OF DOUGLAS M. ALBERT
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

I, Douglas M. Albert, hereby declare as follows:

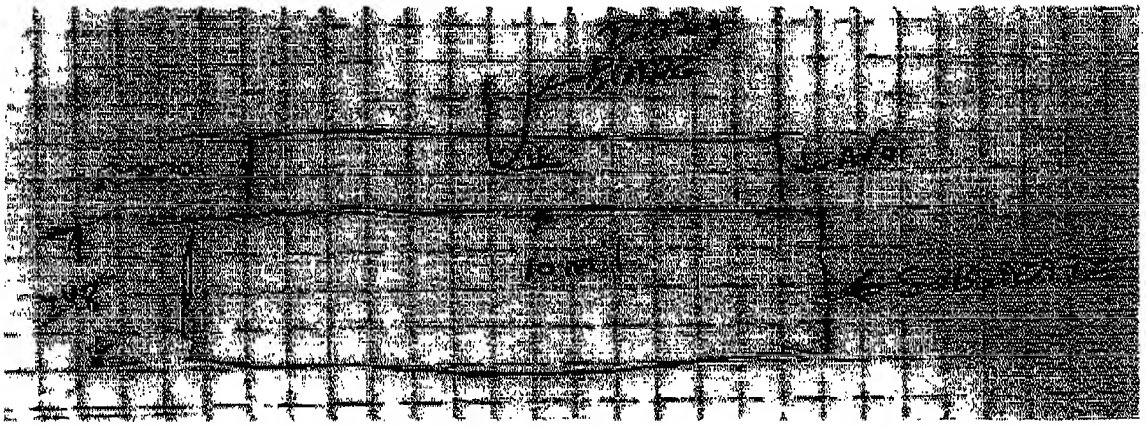
1. I am a co-inventor of the invention disclosed and claimed in patent application no. 09/190,378. I am making this declaration to establish facts showing that the invention claimed in this application was reduced to practice before February 7, 1996, which I am informed is the filing date of the application that issued to Alan J. Riding et al. as U.S. Patent No. 6,083,811 ('811 Patent). I will hereinafter refer to February 7, 1996 as the "Effective Date" of the '811 Patent.

2. I am employed by the assignee, Irvine Sensors Corporation ("ISC"). I work at ISC's Costa Mesa facility in the State of California. I have been employed continuously by ISC at all times relevant hereto

3. I have read Claims 1-32 that are pending in this application and have a technical understanding of how such claims apply to the disclosure of this application. As shown by the exhibits that I have attached hereto, Mr. Ozguz and I developed the method for thinning semiconductor wafers that is described and claimed in our patent application before the Effective Date of the '811 Patent.

4. Attached hereto as Exhibit A, for example, is a page from my inventor's notebook entitled "Grinding with Diced Wafers", dated "7/27/95", which describes and illustrates the claimed invention as follows:

> Theory – Dice wafers <u>partially</u> through leaving 10 mil of [silicon] between bottom of cut and bottom of wafer. After dicing, mount wafer to substrate and grind past depth of dicing cut, therefore leaving chips mounted to substrate as opposed to a wafer.



5. At the bottom of Exhibit A are detailed observations regarding three actual "results", i.e. evidence of an actual reduction to practice of our claimed invention at least as of July 27, 1995, prior to the Effective Date of the '811 Patent.

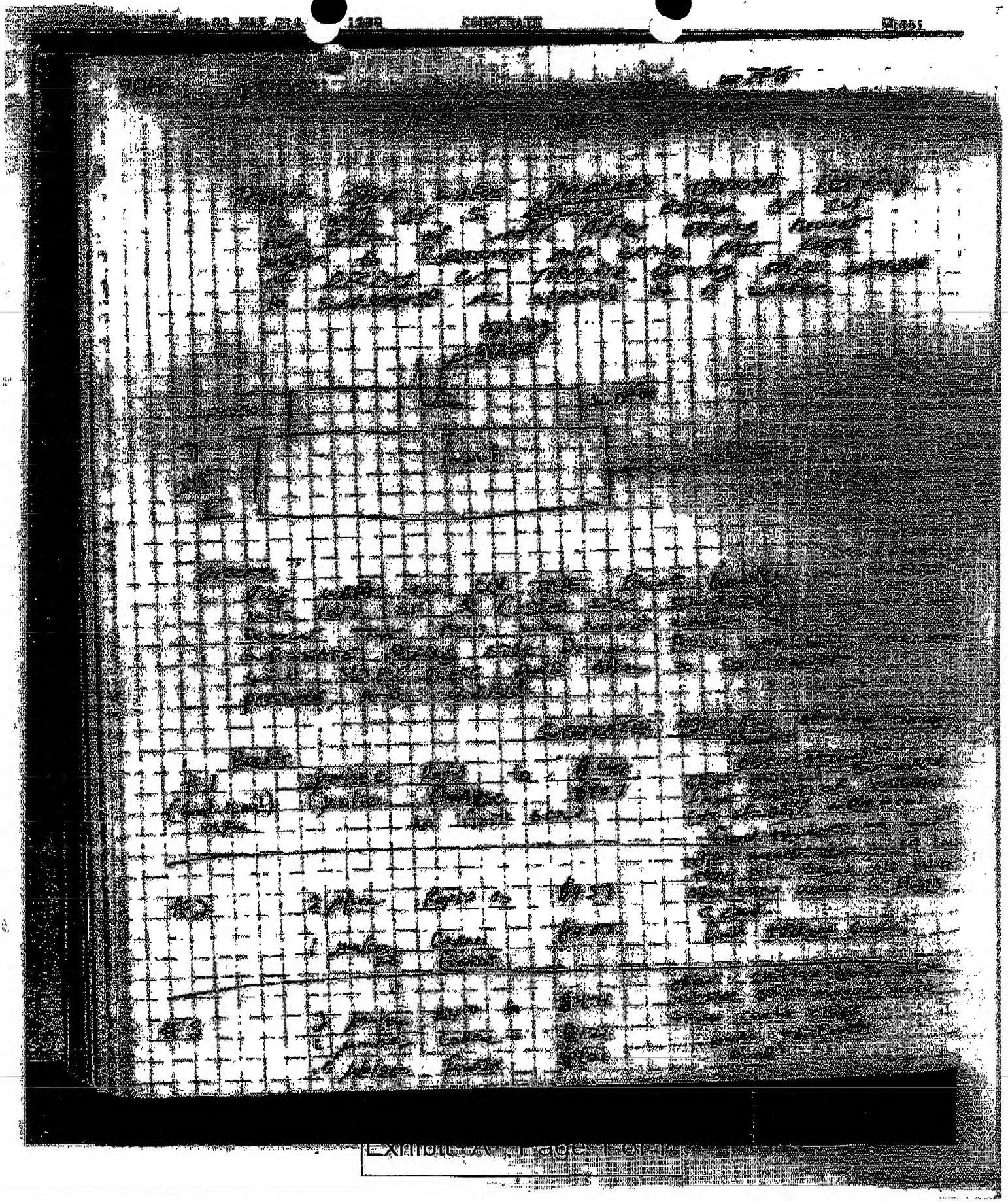
6. Also attached hereto as Exhibit B is a written "Status Report" that I prepared on or about "8-1-95". The memo further corroborates our having successfully back-ground partially diced wafers, in the manner claimed in our patent application, prior to the Effective Date of the '811 Patent.

7. This declaration factually establishes that the claimed invention was reduced to practice in the United States prior to the Effective Date of the '811 Patent.

8. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

10/19/2001
Date

Douglas M. Albert



HDIOI STATUS REPORT

IRVINE SENSORS CORP.

Subject: Present Wafer Thinning Experiment Status
To: Angel Pepe, Dave Ludwig
From: Doug Albert
Date: 8-1-95
CC: K.G., Y.H.

Conclusion:
Based on my experiments up to this point it appears clear to me that in order to ultimately thin wafers to 10 µm a wafer backing medium will be necessary. The challenge I was handed was to see how thin a 5" wafer could be mechanically be ground. Considering there really was no spec. established for mechanical grinding, my goal was to go as thin as possible. The initial thoughts of mounting and grinding wafers on UV tape and processing them on the tape now look dismal. The thinnest wafer that was ground with NO breakage was 4 mils and even that is NOT repeatable. Also, demounting the UV tape from a wafer that is very thin proved very difficult and seems to me a high risk approach.

A second approach was to mount a wafer to a substrate with some sort of adhesive then thin and process the wafer on the substrate. Presently this method is working fairly well. I have been thinning 4" wafers submounted to Macor substrates using a variety of adhesives. I have successfully thinned and demounted 2 mil wafers and ground 1 wafer to 20 µm (not demounted). The process does appear to be pretty repeatable. By far the most touchy area is demounting and propagation of cracking from wafer edge. Note: The program calls for thinning 5" wafers for which the substrates are on order. Until proper substrates are received and tried nothing is for sure.

To go one step further, in order to eliminate crack propagation across a wafer and isolate chips within a substrate a chip isolation process was born. By dicing partially through a wafer, mounting the diced surface down toward the substrate and grinding down past the diced grooves, chips were created hence eliminating crack propagation. This also creates chips alleviating the need to create chips using a lithographic process using plasma etching. I am still working some small movement problems with this process. I am also still establishing my thinning limits with this process as well.

All in all things look positive. I am continuing with experiments and will have a more in depth report upon completion of the experiments. I presently do not see any major roadblocks. I am confident that the present problems can be solved.

Diced Submount Thinning

The next step was to see if we could eliminate the need to dice streets after the thinning in order to create chips. By performing the chip isolation early in the process we now will only lose a chip in the event of a crack or breakage. The way this was performed was to dice partially into a wafer mount the diced side down and backgrind the wafer submounted to the substrate. When the wafer was ground past the depth of the dicing and the grinding was complete you had chips mounted on a substrate. The wax did fill the dicing grooves and acted as a barrier once the grooves were reached from grinding. This reduced edge damage from grinding process. The thinnest I have been able to grind using this method is approx. 4 mils (101μm).

Problems

1. One problem with the thinner wax was chip movement. Reduced feed rates helped slightly.
2. The thicker stronger bond waxes had air pockets and were to viscous thus not allowing good squeeze out of adhesive.
3. The stronger bond adhesives tended to load the grinding wheel.
4. The stronger waxes are slightly harder to demount but not a roadblock.

Docket No. IRV1.PAU.30 **Patent Application**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :	Examiner: D. Graybill
Douglas M. Albert et al.	Group Art Unit: 3722
Serial No.: 09/190,378	
Filed: November 10, 1998	
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine, California
	October 22, 2001

DECLARATION OF INVENTOR VOLKAN H. OZGUZ
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

I, Volkan H. Ozguz, hereby declare as follows:

1. I am an inventor in this application. I am making this declaration to establish facts showing that the invention claimed in this application was reduced to practice before February 7, 1996, which I am informed is the filing date of the application that issued to Alan J. Riding et al. as U.S. Patent No. 6,083,811 ('811 Patent). I will hereinafter refer to February 7, 1996 as the "Effective Date" of the '811 Patent.

2. I am employed by the assignee, Irvine Sensors Corporation ("ISC"). I work at ISC's Costa Mesa facility in the State of California. I have been employed continuously by ISC at all times relevant hereto

3. I have read Claims 1-32 that are pending in this application and have a technical understanding of how such claims apply to the disclosure of this application.

4. As a co-inventor, I actively collaborated with Mr. Albert in the development of the claimed invention and am personally familiar with the development of the invention claimed in our patent application. I have reviewed the fully-executed DECLARATION OF DOUGLAS M. ALBERT SWEARING BEHIND REFERENCE, including Exhibits "A" and "B" attached thereto. I hereby adopt and incorporate by reference the content of paragraphs 4 to 6 of Mr. Albert's declaration and the attached Exhibits "A" and B", as if such descriptions were fully set forth herein and such exhibits were attached hereto.

5. This declaration factually establishes that the claimed invention was reduced to practice in the United States prior to the Effective Date of the '811 Patent.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

10/19/2001.
Date

Volkan H. Ozguz

Atty. Dkt. No.: IRV1.PAU.30 **PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Douglas M. Albert et al.	Examiner:	D. Graybill
Serial No.:	09/190,378	Art Unit:	2814
Filed:	November 10, 1998		
Title:	METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine California October 22, 2001	

REQUEST FOR THREE-MONTH EXTENSION OF TIME

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

Applicants request a three-month extension of time from July 20, 2001 to October 22, 2001 to respond to the Office Action of April 20, 2001.

Our check in the amount of $460.00 to cover the fee for such an extension of time is enclosed.

Please charge any additional fees to our Deposit Account No. 01-1960. One copy of this letter is enclosed for such purpose.

Certificate of Mailing
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on October 22, 2001

By Angela Williams

Signature
October 22, 2001

Respectfully submitted,

Joseph C. Andras
Registration No. 33,469
Myers, Dawes & Andras
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Irvine, CA 92612
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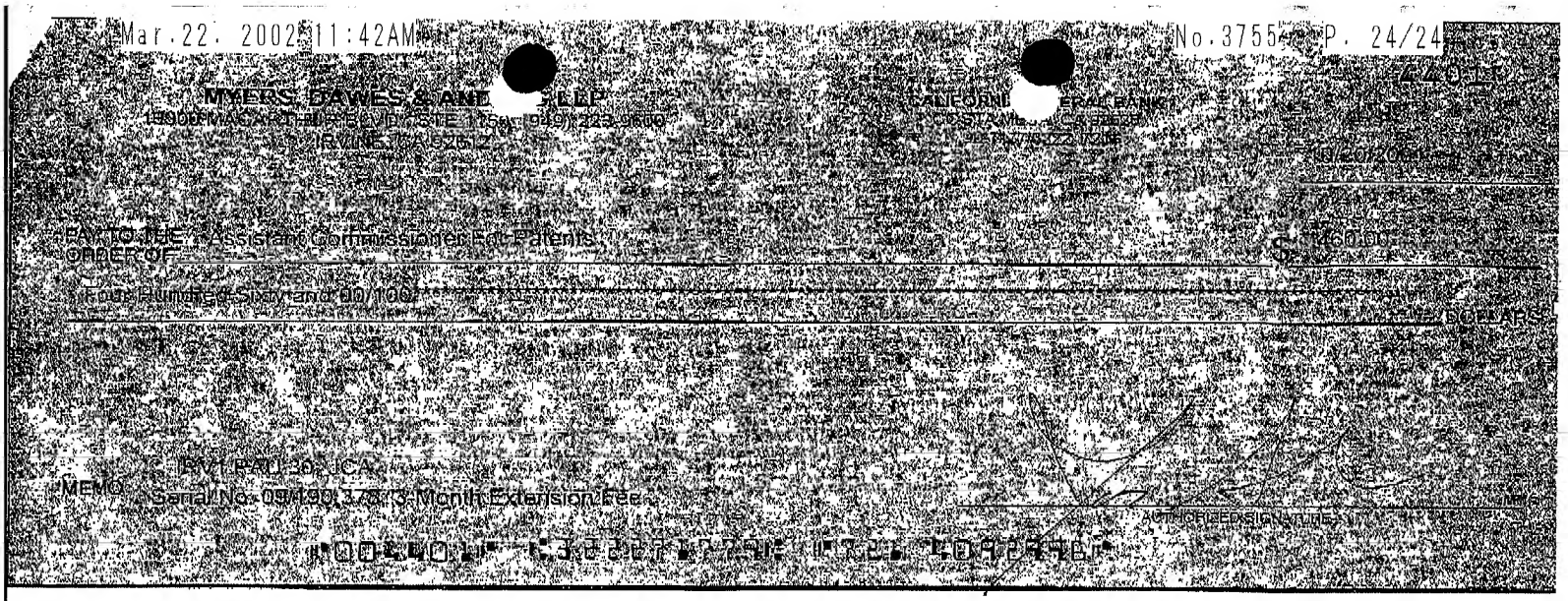

MYERS, DAWES & ANDRAS LLP

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The official stamp of the PTO hereon acknowledges receipt of:

Date: October 22, 2001
Serial No.: 09/190,378